## **Memory Aggregation For KVM**

Hecatonchire Project

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## Agenda



- Memory as a Utility
- Raw Performance
- First Use Case : Post Copy
- Second Use case : Memory aggregation
- Lego Cloud
- Summary



## Memory as a Utility

### How we Liquefied Memory Resources





The Idea: Turning memory into a distributed memory se



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## **High Level Principle**





### How does it work (Simplified Version)









### Full Linux MMU integration (reducing the system-wide effects/cost of page fault)

- Enabling to perform page fault transparency (only pausing the requesting thread)

## Low latency RDMA Engine and page transfer protocol (<u>reducing latency/cost of page faults</u>)

- Implemented fully in kernel mode OFED VERBS
- Can use the fastest RDMA hardware available (IB, IWARP, RoCE)
- Tested with Software RDMA solution (Soft IWARP and SoftRoCE) (NO SPECIAL HW REQUIRED)

#### Demand pre-paging (pre-fetching) mechanism (reducing the number of page faults)

- Currently only a simple fetching of pages surrounding page on which fault occurred



### Minimal Modification of the kernel (simple and minimal intrusion)

• 4 Hooks in the static kernel , virtually no overhead when enabled for normal operation

#### Paging and memory Cgroup support (<u>Transparent Tiered Memory</u>)

 Page are pushed back to their sponsor when paging occurs or if they are local they can be swapped out normally

### KVM Specific support (Virtualization Friendly)

- Shadow Page table (EPT / NPT )
- KVM Asynchronous Page Fault

## Transparent Solution (cont.)



### Scalable Active - Active Mode (Distributed Shared Memory)

Shared Nothing with distributed index

Write invalidate with distributed index (end of this year)

### Library LibHeca (Ease of integration)

Simple API bootstrapping and synching all participating nodes

### • We also support:

- KSM
- Huge Page
- Discontinuous Shared Memory Region
- Multiple DSM / VM groups on the same physical node



## **Raw Performance**

How fast can we move memory around ?





## **Raw Bandwidth usage**



HW: 4 core i5-2500 CPU @ 3.30GHz- SoftIwarp 10GbE - Iwarp Chelsio T422 10GbE - IB ConnectX2 QVA 40 Gbps



## Hard Page Fault Resolution Performance



	Resolution time Average (µs)	Time spend over the wire one way Average (μs)	Resolution time Best (µs)
SoftIwar p (10 GbE)	355	150 +	74
lwarp (10GbE)	48	4-6	28
Infiniban d (40	29	2-4	16

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![](_page_13_Picture_0.jpeg)

## **Post-Copy Live Migration**

Technology first Use Case

![](_page_13_Picture_3.jpeg)

![](_page_13_Picture_4.jpeg)

## Post Copy - Pre Copy - Hybrid Comparison

![](_page_14_Figure_1.jpeg)

![](_page_15_Figure_0.jpeg)

## **Post Copy Migration of HANA DB**

![](_page_16_Picture_1.jpeg)

		Baselin e	Pre-Copy	Post- Copy	
	Downtime	N/A	7.47 s	675 ms	
	Benchmark Performanc e Degradatio	0%	Benchma rk Failed	5%	
Virtua  • 10 0	I Machine: GB Ram , 4 vCPU ication : HANA ( In memo	ry	Hardware: •Intel(R) Core(TM) i5-25 16GB RAM	00 CPU @ 3.30GHz, 4 d	cores,

Database)

Fabric: 10 GB Ethernet Switch

NIC: Chelsio IWARP T422-CR

![](_page_17_Picture_0.jpeg)

## **Memory Aggregation**

Second use case: Scaling out Memory

![](_page_17_Picture_3.jpeg)

![](_page_17_Picture_4.jpeg)

## Scaling Out Virtual Machine Memo

### **Business Problem**

 Heavy swap usage slows execution time for data intensive applications

### **Hecatonchire/ RRAIM Solution**

- Applications use memory mobility for high performance swap resource
  - Completely transparent
  - No integration required
  - Act on results sooner
  - High reliability built in
- Enables iteration or additional data to improve results

![](_page_18_Figure_10.jpeg)

# Redundant Array of Inexpensive Reference Refer

![](_page_19_Figure_1.jpeg)

- 1. Memory region backed by two remote nodes. Remote page faults and swap outs initiated simultaneously to all relevant nodes.
- 2. No immediate effect on computation node upon failure of node.

![](_page_19_Picture_4.jpeg)

### **Quicksort Benchmark with Memory Constraint**

![](_page_20_Picture_1.jpeg)

![](_page_20_Figure_2.jpeg)

3:4	2.08%	5.21%
1:2	2.62%	6.15%
1:3	3.35%	9.21%
1:4	4.15%	8.68%
1:5	4.71%	9.28%

![](_page_20_Figure_4.jpeg)

## Scaling out HANA

![](_page_21_Picture_1.jpeg)

#### DSM RRAIM Memor y Ratio **Overhe Overhe** ad ad 1:2 1% 0.887% 1.548% 1:31.6% 2:1:1 0.1% 1:1:1 1.5%

![](_page_21_Figure_3.jpeg)

#### Virtual Machine:

- 18 GB Ram , 4 vCPU
- Application : HANA ( In memory Database )
- Workload : SAP-H ( **TPC-H** Variant)

#### Hardware:

 Memory Host: Intel(R) Core(TM) i5-2500 CPU @ 3.30GHz, 4 cores, 16GB RAM

•Compute Host: Intel(R) Xeon(R) CPU X5650 @ 2.56GHz, 8 cores, 96GB RAM

Fabric: Infiniband **QDR 40Gbps** Switch + Mellanox ConnectX2

## Transitioning to a Memory Cloud (Ongoing work)

![](_page_22_Figure_1.jpeg)

![](_page_23_Picture_0.jpeg)

## Lego Cloud

Going beyond Memory

![](_page_23_Picture_3.jpeg)

![](_page_23_Picture_4.jpeg)

### Virtual Distributed Shared Memory System (Compute Cloud)

#### **Compute aggregation**

 Idea : Virtual Machine compute and memory span Multiple physical Nodes

#### Challenges

- Coherency Protocol
- Granularity (False sharing)

#### **Hecatonchire Value Proposition**

- Optimal price / performance by using commodity hardware
- Operational flexibility: node downtime without downing the cluster
- Seamless deployment within existing cloud

![](_page_24_Figure_10.jpeg)

## **Disaggregation of datacentre ( and cloud ) resources**

(Our Aim)

Breaking out the functions of Memory ,Compute, I/O, and optimizing the delivery of each.

### Disaggrepation provides three primary benefits:

- Each function is isolated => limiting the scope of what each box must do
- We can leverage dedicated hardware and software => increases performance.

### Superior Scalability:

- Functions are isolated from each other
  => alter one function without impacting the others.
- Improved Economics:
  - cost-effective deployment of resource
    => improved provisioning and
    consolidation of disparate equipment

![](_page_25_Figure_10.jpeg)

![](_page_26_Picture_0.jpeg)

## Summary

![](_page_26_Picture_2.jpeg)

![](_page_26_Picture_3.jpeg)

## **Hecatonchire Project**

![](_page_27_Picture_1.jpeg)

### - Features:

- Distributed Shared Memory
- Memory extension via Memory Servers
- HA features
- Future :Distributed Workload executions
  - Use standard Cloud interface
  - Optimise Cloud infrastructure
  - Support COTS HW

## Key takeaways

- Hecatonchire project aim at disaggregating datacentre resources
- Hecatonchire Project currently deliver memory cloud capabilities
- Enhancements to be released as open source under GPLv2 and LGPL licenses by the end of November 2012
- Hosted on GitHub, check: <u>www.hecatonchire.com</u>
- Developed by SAP Research Technology Infrastructure (TI) Programme

![](_page_28_Picture_7.jpeg)

![](_page_28_Picture_8.jpeg)

![](_page_29_Picture_0.jpeg)

![](_page_29_Picture_1.jpeg)

## Thank you

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## **Backup Slide**

![](_page_30_Picture_1.jpeg)

![](_page_30_Picture_2.jpeg)

### **Instant Flash Cloning On-Demand**

#### **Business Problem**

- Burst load / service usage that cannot be satisfied in time

#### **Existing solutions**

- Vendors: Amazon / VMWare/ rightscale
- Startup VM from disk image
- Requires full VM OS startup sequence

#### **Hecatonchire Solution**

- Go live after VM-state (MBs) and hot memory (<5%) cloning
- Use post-copy live-migration schema in background
- Complete background transfer and disconnect from source

#### **Hecatonchire Value Proposition**

- Just in time (sub-second) provisioning

![](_page_31_Picture_13.jpeg)

### **DRAM Latency Has Remained Constant**

CPU clock speed and memory bandwidth increased steadily (at least until 2000)

But memory latency remained constant – so local memory has gotten slower from the CPU perspective

![](_page_32_Figure_4.jpeg)

Source: J. Karstens: In-Memory Technology at SAP. DKOM 2010

![](_page_32_Picture_6.jpeg)

### **CPUs Stopped Getting Faster**

Moore's law prevailed until 2005 when core's speed hit a practical limit of about 3.4 GHz

Since 2005 you do get more cores but the "single threaded free lunch" is over

Effectively arbitrary sequential algorithms have not gotten faster since

2.000 1.000 Ο CK ICON to ad **e** 2000 19 Year The free lunch is so over multi single-threaded free lunch core 1990s 2010s 1975 2005 2011 Source: "The Free Lunch Is Over.." by Herb Sutter

![](_page_33_Picture_5.jpeg)

![](_page_33_Figure_6.jpeg)

![](_page_33_Picture_7.jpeg)

### While ... Interconnect Link Speed has Kept Growing

![](_page_34_Picture_1.jpeg)

Ethernet (1979 - )	10 Mbit/sec	
Fast Ethernet (1993 -)	100 Mbit/sec	
Gigabit Ethernet (1995 -)	1000 Mbit /sec	
ATM (1995 -)	155/622/1024 Mbit/sec	
Myrinet (1993 -)	1 Gbit/sec	
Fibre Channel (1994 -)	1 Gbit/sec	
InfiniBand (2001 -)	2 Gbit/sec (1X SDR)	
10-Gigabit Ethernet (2001 -)	10 Gbit/sec	
InfiniBand (2003 )	8 Gbit/sec (4X SDR)	
InfiniBand (2005 -)	16 Gbit/sec (4X DDR)	
	24 Gbit/sec (12X SDR)	
InfiniBand (2007 -)	32 Gbit/sec (4X QDR)	
40-Gigabit Ethernet (2010 -)	40 Gbit/sec	
InfiniBand (2011 -)	56 Gbit/sec (4X FDR)	
InfiniBand (2012 -)	100 Gbit/sec (4X EDR)	

Panda et al. Supercomputing 2009

### **Result: Remote Nodes Have Gotten Closer**

![](_page_35_Picture_1.jpeg)

Accessing DRAM on a remote host via IB interconnects is only 20x slower than local DRAM

And remote DRAM has far better performance than paging in from an SSD or HDD device

Fast interconnects have become a commodity - moving out of the High Performance Computing (HPC) niche

![](_page_35_Figure_5.jpeg)

### **Post-Copy Live Migration (pre-migration)**

![](_page_36_Picture_1.jpeg)

![](_page_36_Figure_2.jpeg)

![](_page_36_Figure_3.jpeg)

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### **Post-Copy Live Migration (reservation)**

![](_page_37_Picture_1.jpeg)

![](_page_37_Figure_2.jpeg)

![](_page_37_Figure_3.jpeg)

### **Post-Copy Live Migration (stop and copy)**

![](_page_38_Picture_1.jpeg)

![](_page_38_Figure_2.jpeg)

![](_page_38_Figure_3.jpeg)

### **Post-Copy Live Migration (post-copy)**

![](_page_39_Picture_1.jpeg)

![](_page_39_Figure_2.jpeg)

![](_page_39_Figure_3.jpeg)

### **Post-Copy Live Migration (commit)**

![](_page_40_Picture_1.jpeg)

![](_page_40_Figure_2.jpeg)

![](_page_40_Figure_3.jpeg)